REMARKS

Claims 1-26 are currently pending in the subject application, and are presently under consideration. Claims 1-9, 11-22 and 24-26 are rejected. Claims 10 and 23 have been indicated as allowable. Claims 1, 3, 11, 16 and 19 have been amended. Claims 3 and 11 have been amended to correct typographical errors and do not further limit the claims. Claim 23 has been cancelled and claim 27 has been added. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

Applicant's representative would like to thank the Examiner for taking the time on August 16, 2005 to discuss the rejection of the claims of the present application, and in particular the cited Allen reference.

I. Rejection of Claims 1-7, 12-22 and 24-26 Under 35 U.S.C. §102(b)

Claims 1-7, 12-22 and 24-26 stand rejected under 35 U.S.C. §102(b) as being anticipated by Allen, U.S. Patent 6,151,568 ("Allen"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 1 has been amended to further clarify the predetermined power characterization and recites that the predetermined power characterization is predetermined based on analyzing power consumption for various associated output loads for the at least one non-conventional circuit to determine a relationship of power as a function of output drive load.

Claim 16 has been amended to further clarify the predetermined power characterizations and recites that the predetermined power characterizations are predetermined based on analyzing power consumption for various associated output loads for each of a given non-conventional circuit type to determine a relationship of power as a function of output drive load for each non-conventional circuit type.

The Examiner cites column 13, line 19 through column 16, line 8 of Allen as anticipating claims 1-7, 12-22 and 24-26. This recitation of Allen appears to disclose matching power modules with components in a power netlist for determining power associated with circuit

components. Allen states that "the power estimation module 76 uses the power netlist and the chosen technology implementation, whether from the technology file, the user-defined technology library, the default or interactively chosen by the user to calculate power." (Col. 13, ll. 57-61) However, Allen et al. is silent on the specifics of how the power is determined for each circuit component, and how any power characterization is predetermined.

Allen also discloses a technique for calculating dynamic power by calculating the capacitance, area, length and activity factor of the net, with the net including intermodule nets, intraoperator nets, and clock nets. A clock net is defined as a net that drives one or more clock inputs to registers on the chip (Col. 14, ll. 30-39). Allen discloses that to calculate the length of the wire of the clock nets, the power estimation module must also compute a number of buffer cells that will be added to the semiconductor chip design. However, Allen also discloses that the number and kind of buffers is unknown during the power consumption estimation (Col. 15, ll. 5-15). Therefore, Allen does not disclose that power is calculated for a given non-conventional circuit based on a predetermined power characterization where the predetermined power characterization is predetermined based on analyzing power consumption for various associated output loads for the at least one non-conventional circuit to determine a relationship of power as a function of output drive load, as recited in claims 1 and 16. Therefore, Allen does not anticipate claims 1 and 16, and claims 2-7 and 17-18, respectively, which depend therefrom.

Claims 2 and 17 recite that the non-conventional circuit is a clock gater. Claim 5 recites that the plurality of non-conventional circuit types are a plurality of clock gater types.

A clock gater is defined in the specification (page 4, ll. 3-15) of the present application as a circuit which receives a first clock signal and outputs a second clock signal that is a function of the input clock signal, and might perform some function on the clock signal, such as adjusting the pulse width or frequency, so that the output clock signal has different characteristics than the input clock signal. The clock gater is designed to have a low input capacitance, so as not to overload the system clock and have high current drive capabilities to drive clock enabled logic gates. As stated in the specification of the present application, this type of circuit is difficult to simulate and ignored by most analysis tools.

As previously stated, Allen discloses that to calculate the length of the wire of the clock nets, the power estimation module must also compute a number of buffer cells that will be added to the semiconductor chip design, which is unknown during the power consumption estimation. Allen does not disclose that the buffer cells are clock gaters, such that the buffer cells have low input capacitance and high current drive capabilities. Assume arguendo that the buffers cells could be clock gaters, Allen discloses that the number of buffer cells is unknown during power consumption estimation, and thus power estimation could not be performed on the buffer cells if they are unknown during power consumption estimation. Therefore, Allen does not disclose calculating power for a clock gater circuit based on a predetermined power characterization where the predetermined power characterization is predetermined based on analyzing power consumption for various associated output loads to determine a relationship of power as a function of output drive load, as recited in dependent claims 2, 5 and 17.

Claim 12 recites a clock gater calculator that determines power consumed by at least one clock gater in a circuit design employing at least one predetermined characterization that correlates power as a function of output drive load for a given clock gater circuit. Again Allen does not disclose that the buffer cells are clock gaters. Additionally, Allen discloses that the number of buffer cells is unknown during power consumption estimation. Furthermore, Allen does not disclose a clock gater calculator that determines power consumed by at least one clock gater in a circuit design employing at least one predetermined characterization that correlates power as a function of output drive load for a given clock gater circuit, as recited in claim 12. Therefore, Allen does not anticipate claim 12, and 13-15, which depend therefrom.

Claim 19 has been amended to include the elements from allowable claim 23, and claim 23 has been cancelled. Therefore, claim 19 and claims 20-22 and 24-25, which depend therefrom should be allowable.

New claim 27, which depends from claim 1, recites that the at least one non-conventional circuit being a circuit that employs drive fight. The Examiner states that circuits that employ buffers read as circuits that employ drive fight. Applicant's representative respectfully disagrees. The specification (page 3, ll. 25-32 - page 4, ll. 1-2) of the present application recites that drive

fight or logic contention is when one transistor (or transistor network) is driving a node to a first voltage level (*e.g.,* VDD) and another transistor (or transistor network) is driving the node to a second voltage level (*e.g.,* GND), where the stronger (widest) of the two transistors or transistor networks will drive the node overriding the weaker transistor or transistor network. A level shifter may be a circuit that employs drive fight. However, a buffer is not a circuit that employs drive fight. Therefore, Allen does not anticipate claim 27.

For the reasons described above, claims 1-7, 12-22 and 24-27 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

II. Rejection of Claim 11 Under 35 U.S.C. §103(a)

Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Allen in view of Croix, U.S. Patent 6,327,557 ("Croix"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 11 depends from claim 1 and further recites that the predetermined power characterization being determined by analyzing a spice characterization of the given non-conventional circuit to correlate power as a function of output drive load. Claim 11 depends from claim 1, and Croix does not make up for the aforementioned deficiencies of Allen with respect to claim 1. Furthermore, Croix does not teach or suggest that the spice characterization of the given non-conventional circuit is analyzed to correlate power as a function of output drive load to determine a predetermine power characterization. Therefore, neither Allen nor Croix alone or in combination teach or suggest claim 11.

For the reasons described above, claim 11 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

III. Rejection of Claim 11 Under 35 U.S.C. §103(a)

Claims 8-9 stand(s) rejected under 35 U.S.C. §103(a) as being unpatentable over Allen in view of Jyu, U.S. Patent No. 5,880,967 ("Jyu"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 8-9 depend indirectly from claim 1. Jyu does not make up for the aforementioned deficiencies of Allen with respect to claim 1. Therefore, neither Allen nor Jyu alone or in combination teach or suggest claims 8 and 9.

For the reasons described above, claims 8-9 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,

Date 8/23/05

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